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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,265	04/02/2004	Fouad A. Faour	10030219-1	1790

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EXAMINER	
VERBITSKY, GAIL KAPLAN	
ART UNIT	**PAPER NUMBER**
2859	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,265	FAOUR ET AL.	
	Examiner	Art Unit	
	Gail Verbitsky	2859	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 7-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 7-17 are finally rejected under 35 U.S.C. 103(a) as being unpatentable over US 5639163 A (Davidson, Evan Ezra et al., hereinafter DAVIDSON) in view of PRIOR ART by DENG (U.S. 6911861) [hereinafter Prior Art].

DAVIDSON discloses or suggests an integrated circuit as claimed by Applicant in Claims 1-3, 7-17 comprising:

Regarding Claim 1: DAVIDSON discloses an integrated circuit comprising

a number of pads;

a constant current source (power supply, Fig. 2) to provide a current I1;

a thermal diode D1 that receives said current I1, said thermal diode being coupled between first C4A and second (ground pad, not explicitly shown) ones of said pads;

an analog to digital converter 36 to

i) receive a forward bias voltage (V1) of the thermal diode D1 (Col. 2, Lines 49-51), and

ii) output (to microprocessor 37, Col. 3, Lines 61-64) a digital representation of the forward bias voltage (V2 -V1).

Regarding Claim 7: DAVIDSON discloses an integrated circuit comprising

a constant current source to provide first and second currents of different magnitudes;

first D1 and second D2 thermal diodes that respectively receive said first I1 and second I2 currents;

a comparator 32 (Fig. 3) to receive forward bias voltages of each of the thermal diodes, to compare the forward bias voltages, and to output a voltage difference indicative of a temperature of the integrated circuit.

Further regarding Claims 2-3 and 17: DAVIDSON discloses logic 37 to receive the digital representation of the forward bias voltage and calculate a temperature of the integrated circuit (Col. 3, Lines 50-52; and Col. 4, Lines 1-4), wherein said logic comprises a temperature look-up table 39 as claimed by Applicant in Claims 3 and 17.

Further regarding Claims 1, 7; DAVIDSON discloses a third one of said pads is provided to receive a reference current, said third pad C4B being coupled to an input of said constant current source as claimed by Applicant. Davidson does not explicitly teach a reference current circuit coupled to the third pad.

Further regarding Claims 8-10 and 16: DAVIDSON discloses the thermal diodes are positioned adjacent one another (Col. 2, Lines 45-49) as claimed by Applicant in Claim 8, and the first and second currents have a known relationship as claimed by Applicant in Claims 9 and 16, and further regarding Claim 10, the second current I2 Is an integer multiple of the first current I1 (Col. 3, Lines 6-15; e.g., a ratio of 100:1).

Further regarding Claim 11: DAVIDSON discloses the comparator 32 is a differential amplifier.

Further regarding Claims 12 and 14: DAVIDSON discloses the integrated circuit further comprising an analog to digital converter 36 to

i) receive the voltage difference output by the differential amplifier, and

ii) output a digital representation of the voltage difference.

Further regarding Claims 13 and 15: DAVIDSON discloses the integrated circuit further comprising logic 37 to receive the digital representation of the voltage difference and calculate a temperature of the integrated circuit.

DAVIDSON, to summarize, discloses or suggests all the limitations as claimed by Applicant in Claims 1-3, 7-17, as described above, except DAVIDSON'S power supply Vp is off the "chip area" as indicated by chip 12 (Fig. 12), therefore is not considered to be a pad of the integrated circuit disclosed by DAVIDSON. DAVIDSON as described above, Davidson does not explicitly teach a reference current circuit coupled to the third pad, and that the said reference current thereby serving to control the constant current source.

Prior Art discloses in Fig. 1 a device in the field of applicant's endeavor comprising a current generating circuit 104 generating a current proportional to a reference current being regulated (controlled/ adjusted) by a resistor (variable current reference, thus, adjusting the constant current source to a device of interest) coupled to the circuit by means of a (third) pad 108.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device, disclosed by Davidson, so as to add a reference current by means of a third pad to a current source, disclosed by Prior Art, in order to generate a current proportional to a temperature, as taught by Prior Art, so as to obtain more accurate results by varying current proportionally to temperature change in the IC, as very well known in the art.

2. Claims 4 and 19 are finally rejected under 35 U.S.C. 1O3(a) as being unpatentable over DAVIDSON and PRIOR ART as applied to claims 1-3, 7-17 above, and further in view of US 6453218 B1 (Vergis, George, hereinafter VERGIS).

DAVIDSON and PRIOR ART, to summarize, disclose or suggest all the limitations as claimed by Applicant in Claims 4 and 19, as described above in Paragraph 9 as applied to Claims 1-3, 7-17 and 20 further including the limitations that the microprocessor 37 has an input that receives the digital representation of the differential input voltage, the digital representation of the voltage difference (between the two forward bias voltages) as claimed by Applicant, and includes a look-up table for converting those values to temperature values, and the microprocessor 37 outputs these values over a suitable bus 41. DAVIDSON discloses that the microprocessor 37 may compare the measured value to a limit and provide an over-temperature output signal to a lead 40 (Col. 3, Line 61 - Col. 4, Line 8).

They as described above, do not explicitly disclose a register to store the digital representation of the forward bias voltage, the digital representation of the voltage difference as claimed by Applicant, said register being readable during normal operation of the integrated circuit as claimed by Applicant.

VERGIS discloses it is known in the art to store the digital representation of a temperature that is based on the forward bias voltage across a diode in a register area 1 04 (Col. 3, Lines 15-33). VERGIS further discloses that it is advantageous to store the digital representation of temperature in a register in order to benefit from the ability to periodically store the data as it is measured, but only read it at convenient times that will

not interfere with other processor operations (Col. 3, Lines 34-54).

VERGIS is evidence that ordinary workers in the field of temperature measurement in integrated circuits would recognize the benefit of adding a register being readable during normal operation of the integrated circuit as taught by VERGIS for the device of DAVIDSON and Prior ART in order to benefit from not interfering with other processor operations by allowing the microprocessor to choose when the temperature data will be transmitted.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute a register being readable during normal operation for the transmitted output signal of DAVIDSON and PRIOR ART in order to not interfering with other processor operations by allowing the microprocessor to choose when the temperature data will be transmitted as taught by VERGIS.

3. Claim 18 is finally rejected under 35 U.S.C. 1O3(a) as being unpatentable over DAVIDSON and PRIOR ART as applied to claims 1-3, 7-17 above and further in view of US 5195827 A (AUDY; Jonathan M. et al., hereinafter AUDY).

DAVIDSON and PRIOR ART, to summarize, disclose or suggest all the limitations as claimed by Applicant in Claim 18, as described above in Paragraph 9 as applied to Claims 1-3, 7-17 and 20 further including the limitations of one analog to digital converter 36 receiving the output of comparator 32. DAVIDSON further disclosed that the currents should be precisely controlled by selecting external resistors with precisely known values.

They as described above, do not explicitly disclose one or more analog to, digital converters receiving the first and second currents and outputting digital representations of said currents to logic.

AUDY discloses an ammeter 24 and analog to digital converter 38 for providing the current data to the central processor 36.

AUDY is evidence that ordinary workers in the field of semiconductor device temperature sensing would recognize the benefit of using an analog to digital converter as taught by AUDY for the precisely known resistors of DAVIDSON and PRIOR ART in order to measure the currents for better accuracy without requiring the resistors.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute an analog to digital converter for the precise resistors controlling the current of DAVIDSON and PRIOR ART in order to use multiple excitations and cancel parasitic base and emitter resistances as taught by AUDY.

Response to Arguments

4. Applicant's arguments filed 01/22/2007 have been fully considered but they are not persuasive. Applicant states that Davidson cannot be combined with Deng. This argument is not persuasive because: A) the Examiner recognizes that there should be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). The test for combining references is what the combination of disclosures taken as a whole would suggest to one od ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971. The references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA) 1969.

B) Davidson discloses all the subject matter as claimed by applicant with the exception of means for regulating a constant current. Deng discloses a device in the field of

applicant's endeavor comprising means for regulating the constant current by means of a pad/ contact/ electrical connection.

C) it is very well known in the art that any current needs and can be regulated depending on a circuit it supplies.

Applicant questions how the circuit of Davidson will operate in combination with the constant current regulator of Deng to come to the claimed invention. In response to this please note, A) the references are from the same field of endeavor as the applicant's invention, B) neither Davidson or Deng teach anything in their disclosures that would suggest that the two are not combinable. C) Davidson does not rule out having a constant current regulator. If, for example, Davidson teaches some specific current value that is out of limit of capability of the constant current regulator of Deng, then the Examiner would agree with the arguments. However, neither references, nor the Applicant disclose specific operation values of the circuits that could question a success of the combination by the Examiner.

The Examiner's position is that the Examiner provided the Applicant with the combination of the references clearly showing the reference current circuit coupled to the constant current circuit to control it and to provide the reference current, as very well known in the art of measuring temperature in IC whose output signal can be temperature dependent and thus, inaccurate.

Conclusion

5. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art cited in the PTO-892 and not mentioned above disclose related devices and methods.

Pippin (U.S. 5838578) discloses in Fig. 10 a temperature sensor implemented in an IC (MP), the IC comprises an on-chip constant current source 140.

Lipp (U.S. 4165642) discloses in Fig. 1 an on-chip temperature sensor, and an ADC located on the same chip 10.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gail Verbitsky whose telephone number is 571/ 272-2253. The examiner can normally be reached on 7:30 to 4:00 ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on 571/ 272-2245. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GKV

Gail Verbitsky
Primary Patent Examiner, TC 2800

March 23, 2007